

**What Is Claimed Is:**

1. A method for characterizing device mismatch in a semiconductor integrated circuit, comprising the steps of:

5 obtaining DC voltage characteristic data for a pair of semiconductor devices; and

processing the DC voltage characteristic data to determine a distribution of device mismatch between devices comprising the device pair.

10 2. The method of claim 1, wherein the device pair comprises two transistors.

3. The method of claim 2, wherein the distribution of device mismatch comprises a distribution of  $V_t$  (threshold voltage) mismatch.

15 4. The method of claim 1, wherein the step of obtaining DC voltage characteristic data for the device pair comprises retrieving said data from a database.

20 5. The method of claim 1, wherein the step of obtaining DC voltage characteristic data for the device pair comprises measuring subthreshold DC voltage characteristic data in a subthreshold region of transistors comprising the device pair.

6. The method of claim 1, wherein the step of obtaining DC voltage characteristic data for the device pair comprises separately measuring DC voltage characteristic data for each of a plurality of similar device pairs.

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7. The method of claim 1, further comprising the step of determining a variation in a device characteristic for a device of an integrated circuit comprising the device pair the distribution of variation of device mismatch for the device pair.

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8. The method of claim 8, further comprising the step of assessing random variation of device mismatch of the semiconductor integrated circuit using variations in the device characteristic for each device of the integrated circuit as determined from distributions of variation of device mismatch for device pairs within the integrated circuit.

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9. The method of claim 8, wherein the device characteristic comprises threshold voltage and wherein the devices comprise transistors.

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10. A method for characterizing device mismatch in a semiconductor integrated circuit, comprising the steps of:

obtaining DC voltage characteristic data for one or more selected device pairs of an integrated circuit, wherein  
5 the device pairs comprise pairs of neighboring transistors in the integrated circuit;

determining a distribution of  $V_t$  (threshold voltage) mismatch for a selected device pair using corresponding DC voltage characteristic data for the device pair;

10 determining a  $V_t$  variation of transistors in the integrated circuit using one or more determined distributions of  $V_t$  mismatch for selected device pairs; and

characterizing random variations of the integrated circuit using one or more determined  $V_t$  variations of  
15 transistors of the integrated circuit.

11. The method of claim 10, wherein the step of obtaining DC voltage characteristic data for a selected device pair of an integrated circuit comprises obtaining subthreshold DC voltage characteristic data while biasing  
20 the transistors of the device pair in a subthreshold region.

12. The method of claim 10, wherein the step of obtaining DC voltage characteristic data for a selected device pair comprises separately measuring DC voltage

characteristic data for each of a plurality of similar device pairs.

13. The method of claim 10, wherein the step of obtaining DC voltage characteristic data for a selected  
5 device pair comprises:

(i) serially connecting a first transistor and a second transistor;

(ii) applying a first gate voltage to a gate of the first transistor and a second gate voltage to a gate of the  
10 second transistor such that the first and second transistors are biased in a subthreshold voltage region, wherein at least one of the first and second gate voltages comprises a varying input voltage;

(iii) determining output voltage of a node between the  
15 first and second transistors as a function of the varying input voltage; and

(iv) repeating steps (i) - (iii) for each of a plurality of separate device pairs of the first and second transistors.

20 14. The method of claim 13, wherein at least one of the first and second gate voltages comprises a constant input voltage to maintain the respective transistor in the subthreshold region.

15. The method of claim 13, wherein the step of  
determining a distribution of  $V_t$  mismatch for the selected  
device pair using the corresponding DC voltage  
characteristic data for the device pair, comprises the steps  
5 of:

determining a distribution of  $V_{IN}$  for a given output  
voltage,  $V_{OUT}$ ; and

determining a distribution of  $V_t$  mismatch of the first  
and second transistors from the distribution of  $V_{IN}$ .

10 16. The method of claim 15, wherein the distribution  
of  $V_{IN}$  corresponds to a distribution of  $V_t$  mismatch between  
the first and second transistors when the first and second  
transistors each comprise an NFET.

15 17. The method of claim 15, wherein the distribution  
of  $V_{IN}$  corresponds to a distribution of one-half the  $V_t$   
mismatch between the first and second transistors when the  
first and second transistors comprise an NFET and PFET.

18. The method of claim 10, wherein the integrated  
circuit comprises an SRAM (static random access memory)  
20 cell.

19. The method of claim 10, wherein the step of determining a  $V_t$  variation of transistors in the integrated circuit comprises determining a standard deviation of  $V_t$  variation of the transistors.

5           20. A testing apparatus for characterizing device mismatch in a semiconductor integrated circuit, comprising:  
            a plurality of test circuits, wherein each test circuit is configured for obtaining subthreshold DC voltage characteristic data for a device pair of an integrated  
10           circuit; and  
            a multiplexer, for selectively outputting an output voltage from each test circuits.

21. The testing apparatus of claim 20, wherein a portion of the plurality of test circuits are configured for  
15           testing the same device pair.

22. The testing apparatus of claim 20, wherein the plurality of test circuits are divided into groups of test circuits, wherein each group of the test circuits comprises the same test circuits.

23. The testing apparatus of claim 20, wherein each group of test circuits is associated with a multiplexer, wherein the multiplexers are controlled such that the output voltages from similar test circuits in each group are simultaneously measured.

24. The testing apparatus of claim 20, further comprising a database for storing the subthreshold DC voltage characteristic data.

25. The testing apparatus of claim 24, further comprising a processing unit for statistically processing the subthreshold DC voltage characteristic data stored in database for determining a distribution of device mismatch of the integrated circuit.

26. A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for characterizing device mismatch in a semiconductor integrated circuit, the method steps comprising:

obtaining DC voltage characteristic data for a pair of semiconductor devices; and

processing the DC voltage characteristic data to determine a distribution of device mismatch between devices comprising the device pair.

27. A program storage device readable by a machine,  
5 tangibly embodying a program of instructions executable by the machine to perform method steps for characterizing device mismatch in a semiconductor integrated circuit, the method steps comprising:

obtaining DC voltage characteristic data for one or  
10 more selected device pairs of an integrated circuit, wherein the device pairs comprise pairs of neighboring transistors in the integrated circuit;

determining a distribution of  $V_t$  (threshold voltage) mismatch for a selected device pair using corresponding DC  
15 voltage characteristic data for the device pair;

determining a  $V_t$  variation of transistors in the integrated circuit using one or more determined distributions of  $V_t$  mismatch for selected device pairs; and

characterizing random  $V_t$  variation of the integrated  
20 circuit using one or more determined  $V_t$  variations of transistors of the integrated circuit.